REMARKS

The Official Action dated November 30, 2005 has been received and its contents carefully noted. In view thereof, claims 14, 17-19 and 21 have been canceled without prejudice nor disclaimer of the subject matter set forth therein, claim 20 has been amended and new claims 23-29 have been added in order to better define that which Applicant regards as the invention. Accordingly, claims 4-12, 20 and 22-29 are presently pending in the instant application.

Initially, Applicant wishes to acknowledge the Examiner's indication on page 6 of the Office Action that claim 22 is allowable over the prior art of record. In this regard, it is respectfully requested that claim 22 as well as the remaining pending claims of the present application be indicated as being allowable for the reasons discussed hereinbelow and that the application be passed to issue.

With reference now to paragraph 2 of the Office Action, claim 20 has been rejected under 35 U.S.C. §102(a) as being anticipated by U.S. Patent No. 6,603,210 issued to Kishimoto et al. This rejection is respectfully traversed in that the patent to Kishimoto et al. neither discloses nor suggests that which is presently set forth by Applicant's claimed invention.

As can be seen from the foregoing amendments, independent claim 20 has been amended to recite a passive element chip comprising a substrate, an insulating layer having a first surface and a second surface opposite to the first surface, wherein the insulating layer is formed on the substrate and the second surface of the insulating layer is faced to the substrate, an inductor formed on the insulating layer surface by a first metal wire, a first electrode formed on the first surface of the insulating layer, wherein the first electrode is coupled to the inductor, a capacitor formed in the insulating layer by a second metal wire, wherein the capacitor is isolated from the inductor, a second electrode formed on the first

surface of the insulating layer, wherein the second electrode is coupled to the capacitor , a protective film formed on the first surface of the insulating layer, wherein the protective film has a first opening for exposing the first electrode and a second opening for exposing the second electrode, a first wiring pattern formed within the first opening and a second wiring pattern formed within the second opening. Clearly, these features are neither disclosed in nor remotely suggested by the teachings of Kishimoto et al.

Specifically, the patent to Kishimoto et al. fails to disclose or remotely suggest that the inductor, the first electrode, the capacitor, the second metal wire and the protective film as defined in claim 20, as amended. In rejecting Applicant's claimed invention, the Examiner regards the insulator layer 4 in Fig. 1 of Kishimoto et al. as a protective film coinciding with the protective film recited by Applicant's claimed invention. However, as is readily apparent from the teachings of Kishimoto et al., the insulating layer 4 of Kishimoto et al. is not formed on a surface of the moulding resin 9 which is opposite to a surface facing toward the conductive layer 3 but is formed on the surface facing the conductive layer 3 itself. Accordingly, it is respectfully submitted that Applicant's claimed invention as set forth in independent claim 20, as amended, clearly distinguishes over the teachings of Kishimoto et al. and is in proper condition for allowance.

With reference to paragraph 4 of the Office Action, claims 4-12, 14 and 21 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Kishimoto et al. in view of U.S. Patent No. 6,582,991 issued to Maeda et al., U.S. Patent Publication No. 20002/0122244 to Lin et al. and U.S. Patent No. 6,853,559 issued to Panella et al. This rejection is respectfully traversed in that the combination proposed by the Examiner neither discloses nor suggests that which is presently set forth by Applicant's claimed invention. Furthermore, the patents to Maeda et al. and Panella et al. as well as the patent publication to Lin et al. fail to overcome the aforementioned shortcomings associated with the teachings of Kishimoto et al.

Particularly, as noted hereinabove, Kishimoto et al. fails to disclose or remotely suggest the inductor, the first electrode, the capacitor, the second metal wire and the protective film as defined in independent claim 20, as amended.

That is, while the patent to Maeda et al. may teach a multi-chip module having IC chip elements/components wherein the chip components include a variety of active and passive components, this reference clearly fails to overcome the shortcomings associated with Kishimoto et al. discussed in detail hereinabove. Similarly, Lin et al. may teach a multi-chip module having a variety of conventional passive devices/chip components and particularly may teach the chip components/passive device as being formed/diced from a wafer using conventional wafer scale processing, this reference likewise fails to overcome the aforementioned shortcomings associated with Kishimoto et al. and clearly fails to disclose or suggest the passive element chip set forth in independent claim 20.

Likewise, while Panella et al. may teach an IC system integration comprising active/passive IC chip components, this reference fails to render obvious that which is presently set forth by Applicant's claimed invention. Accordingly, in that Kishimoto et al. when taken alone or in view of the combined teachings of Maeda et al., Lin et al. and Panella et al. clearly fail to disclose or remotely suggest that which the passive element chip presently set forth in independent claim 20, it is respectfully submitted that independent claim 20 as well as those claims which depend therefrom clearly distinguish over the combination proposed by the Examiner and are in proper condition for allowance.

Therefore, in view of the foregoing it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner and that claim 22, again, be indicated as being allowable over the prior art of record along with pending claims 4-12, 20, 21 and 23-29, and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,

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